

REMARKS

Applicants respectfully request reconsideration of the present application based on the foregoing amendments and the following remarks. Applicants herein amend claims 1, 5 and 10-13. Claims 1-20 remain pending in the application.

Claim Rejections Under 35 U.S.C. § 103(a)

Claims 1-20 stand rejected under 35 U.S.C. § 103(a) as being obvious in view of U.S. Patent No. 6,587,995 to Duboc et al. ("Duboc"). For reasons set forth more fully below, Applicants respectfully traverse this rejection.

Amended Independent Claims 1 and 13 Patentably Define Over Duboc

Independent claims 1 and 13 have been amended to clarify the usability of the present invention with configurable processors, and to both require that the claimed interpreting agent is able to interpret different state-accessing instruction streams that are prepared for different configurations of a configurable processor. For example, claim 1 has been amended to recite:

preparing a first state-accessing instruction stream based on a first user description of the configurable processor;
transmitting, using a debugger, the first state-accessing instruction stream to an interpreting agent, the interpreting agent being capable of interpreting that stream;
causing, using the first state-accessing instruction stream, the interpreting agent to return the state of a first configuration of the configurable processor to the debugger;
preparing a second different state-accessing instruction stream based on a second different user description of the configurable processor;
transmitting, using the debugger, the second state-accessing instruction stream to the interpreting agent, the interpreting agent also being capable of interpreting that second stream; and
causing, using the second state-accessing instruction stream, the interpreting agent to return the state of a second different configuration of the configurable processor to the debugger

As set forth in the present specification at, for example, page 16, lines 9-15, an aspect of the invention is that different interpreting agents do not have to be built for different processor configurations.

The Office Action acknowledges that Duboc does not describe state-accessing instruction streams at all. Moreover, Duboc's alleged interpreting agent (debug monitor 52) must be specially built for each specification of a processor core (see, e.g., col. 14, lines 53-65). In other words, Duboc requires its monitor and debugger to be "core-specific," (see col. 15, line 3) i.e., the monitor and debugger are specific for a single configuration of a processor. If a new processor is configured, the monitor and debugger must be re-built. Accordingly, the debug monitor 52 is not capable of accessing state for different configurations of a configurable processor as required by amended independent claims 1 and 13.

For at least the above reasons, the rejection of claims 1 and 13, as well as claims 2-8 and 14-20 that depend therefrom, should be withdrawn.

Independent Claim 9 Patentably Defines Over Duboc

Independent claim 9 requires, *inter alia*, a computer readable medium including software for automatically generating a hardware description of a configurable processor from a user description of the processor.

The Office Action alleges that it would be obvious to one skilled in the art to modify Duboc's invention to meet this limitation. However, the Office Action relies on processor design tools, which merely assist a designer in manually generating a hardware description of a processor.

As set forth previously, the present assignee Tensilica has developed highly advanced software programs that allow a designer to specify various features of a processor (e.g. register file sizes, etc.), and then automatically generate hardware descriptions for that configured processor. These products have become well known, as is the term "configurable processor." Duboc does not disclose anything about configurable processors, much less a program that automatically generates a hardware description of a configurable processor based on a user specification. At the time of Duboc's invention (April 2000), it is believed that the only technology permitting the automatic generation of configurable processors would have been

patents and applications related to Tensilica's Xtensa products. However, it would be improper to base an obviousness rejection on the present assignee's own inventions.

For at least the above reasons, the rejection of independent claim 9 should be withdrawn.

Amended Independent Claim 10 and Dependent Claim 11 Patentably Define Over Duboc

Independent claim 10 has been amended to further clarify that the debugger library is includes functionality for generating saving and restoring state instruction streams that are capable of being executed on the configurable processor based on a description of a configurable processor. This feature of the invention allows, for example, save and restore instruction streams to be readily generated and executed on a different versions of a configurable processor.

As set forth above, Duboc merely describes sending "debug parameters" to a debug monitor for configuring certain debugging operations. Duboc does not disclose or suggest anything about save and restore state instructions that can be executed by an embedded processor to access state information, much less a debugger library that can generate such instruction streams based on a user specification of a configurable processor as required by claim 10.

Dependent claim 11 has also been amended to clarify that the state interdependencies are identified for a state that has been added to the configurable processor based on a user description. Nothing in Duboc suggests a debugger library having this capability.

For at least the above reasons, the rejection of claims 10 and 11 should be withdrawn.

Amended Independent Claim 12 Patentably Defines Over Duboc

Independent claim 12 has been amended in a similar manner to claims 1 and 13 and thus require that the claimed instruction-insertion server is capable of interpreting different state-accessing instruction streams for different configurations of a configurable processor. As set forth above, Duboc's monitor 52 is not capable of interpreting instruction streams at all, much less different instruction streams generated for different configurations of a configurable processor.

For at least the above reasons, the § 103 rejection of this claim should be withdrawn.

Claims 3, 7, 15 and 19 Further Patentably Define Over Duboc

Claims 3 and 7 depend from claim 1, and claims 15 and 19 depend from claim 13.

Claims 1 and 13 have been shown above to patentably define over Duboc. Accordingly, claims 3, 7, 15 and 19 are patentable at least due to their dependence from patentable claims 1, 10 and 13.

Claims 3, 7, 15 and 19 require that the interpreting agent is an instruction-insertion server. Contrary to the Office Action, nothing in Duboc suggests an instruction-insertion server that is able to interpret instruction streams and access state from a processor using those streams.

Duboc's monitor 52 is the only mechanism that is alleged to correspond to the claimed interpreting agent. Monitor 52 is either a debug monitor or an instruction server. It cannot be both, and the reliance on passages that merely describe server architectures are not sufficient to meet all the limitations of the claims. Accordingly, the rejection of dependent claims 3, 7, 15 and 19 is further improper for at least the above reasons, and the rejections should be withdrawn.

Conclusion

All objections and rejections having been addressed, and in view of the foregoing, the claims are believed to be in form for allowance, and such action is hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, s/he is kindly requested to contact the undersigned at the telephone number listed below.

Date: March 31, 2005

Respectfully submitted,
PILLSBURY WINTHROP LLP



Mark J. Danielson
(650) 233-4777

40,580

Reg. No.

Please reply to customer no. 27,498